

# Abinash Singh

+916006041324 | abinashsinghalotra@gmail.com |  
linkedin.com/in/abinashsinghalotra | github.com/avinashlalotra  
682022 Kochi India

## SUMMARY

---

I have debugged and resolved issues in over 100 functions and multiple libraries during my time at FOSSEE. This experience has honed my patience and equipped me with strong hands-on debugging skills.

## TECHNICAL SKILLS

---

**Programming Languages:** C/C++, Python, Java, Bash/Shell Scripting

**Development Tools:** Git/GitHub, Docker,

## EXPERIENCE

---

### Intern

FOSSEE, IIT Bombay

September 2024 - Nov 2024

Mumbai, India

- Conducted architectural analysis of Xcos, a Scilab-based modeling and simulation tool, evaluating the feasibility of Octave integration and multi-language support to make Xcos more independent.
- Identified limitations in the existing Scilab-based architecture and provided strategic recommendations to optimize development focus saving months of development time by refocusing the project roadmap
- Designed and implemented new Scicos blocks, contributing to the enhancement of Xcos's modeling and simulation capabilities.
- Ported 19 signal processing functions to Scilab handling complex dependencies and tests.

### Semester-Long Intern

FOSSEE, IIT Bombay

March 2024 – July 2024

Mumbai, India

- Ported the Octave Signal processing library to Scilab, replacing the previous C++ implementation that dynamically linked liboctave with a new, fully native Scilab codebase, resulting in improved integration and performance.
- Debugged and resolved segmentation fault issues in the FSOT toolbox, enhancing stability and reliability.
- Identified and fixed multiple bugs, optimizing performance and reducing memory usage, leading to faster execution times.
- Achieved a performance improvement of up to 50% faster processing for large datasets and complex computations, compared to the previous liboctave-based implementation.
- Reduced memory usage by approximately 100%, making the library more efficient and responsive.
- Collaborated with a team to enhance and publish over 60 functions, ensuring thorough documentation and rigorous testing, significantly improving the toolbox's reliability.
- Introduced new features such as plotting functionality, advanced complex data computations, and support for large matrix handling, which were previously unavailable in Scilab's signal processing library.
- Utilized Scilab, Octave, Git, Linux, shared libraries, linker configuration, and C++ for project management, development, and integration of components.

## PROJECTS

---

### Edge AI Accelerator

Jan 2025 - present  
Verilog, SystemC, RISC-V, FPGA

- Designing a systolic array-based matrix multiplication coprocessor for accelerating edge AI inference on Xilinx FPGAs.
- Modeled and verified MAC units, single-port RAM, and bus interfaces in SystemC, enabling integration with the PicoRV32 RISC-V core.
- Implemented RTL modules in Verilog and validated functionality with testbenches.

### Simple Bootloader

x86 Assembly, BIOS interrupts

- Developed a simple bootloader in assembly language, implementing a print\_string function to output text using BIOS interrupts.

- Assembled and tested the bootloader using NASM and QEMU, gaining practical experience in low-level programming and system architecture.
- Created a Makefile for efficient builds and streamlined the development process, ensuring the bootloader adhered to the 512-byte size constraint.
- Documented the project with a detailed README, providing setup instructions and code explanations to facilitate understanding and usage.

### **PPE Detection System**

November 2023

*Computer Vision Project*

*Python, OpenCV, Roboflow, PyQt5*

- A PPE detection system for the college tech fest "DISHNA," and successfully presented it to BPCL in collaboration with the Department of Fire and Safety Engineering.
- Leveraged pre-trained YOLO weights to create an accurate and efficient object detection model for personal protective equipment (PPE) recognition.
- Implemented a graphical user interface (GUI) using PyQt5 to display detected violations, and demonstrated the system's use cases for remote surveillance and workplace entry control.

### **Open Source Contributions**

- Migrated eSim 2.4 from Ubuntu 18.04 LTS to Ubuntu 22.04 LTS/23.04 .
- Currently collaborating with FOSSEE to package eSim 2.4 for distribution across various Linux distros
- Maintaining Signal Processing toolbox of FOSSEE

## **EDUCATION**

---

**Cochin University of Science and Technology (CUSAT)**

Kochi, India

*B.tech in Electronics and Communication Engineering*

*September 2022 – July 2026*

**PMUSPY SSSJKL Scholar**

Session 2022-2023

## **CERTIFICATIONS**

---

- Deep Learning Specialization
- Embedded Linux and Buildroot

## **HACKATHONS AND EVENTS**

---

- Make-a-ton 7.0 "Change Maker" track winner
- Code reCET at CET Trivandrum First Prize
- INKRIT 2.0 at MES College Aluva First Prize
- Magnathon 2.0 IEEE student branch College of Engineering Vadakara Team 2nd Runner-up
- Among top 15 in GDSC CUSAT data structures and algorithms Learning Series
- Innovation and Design Boot Camp participant (IEDC Phase II)